UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,417	03/02/2004	Wan Yen Teoh	03-11	5407

22443 7590 05/02/2006

LAW OFFICE OF MONICA H CHOI
P O BOX 3424
DUBLIN, OH 430160204

EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

E

Office Action Summary	Application No.	Applicant(s)	
	10/791,417	TEOH ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/791,417 has a total of 20 claims pending in the application, there are 2 independent claims and 18 dependent claims, all of which are ready for examination by the Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by the Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted March 2, 2004 are acceptable for examination purposes.

OBJECTIONS

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Cycling Through Addresses Of A Flash Memory Device Using A Gray Code Bit Pattern Sequence."

Claims

4. **Claim 17** is objected to because of the following informalities: On line 1 the word "mean" should read "means."

Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being obvious over Lee et al. "Mobile Ion-Induced Data Retention Failure in NOR Flash Memory Cells" in view of Okazawa (U.S. Patent 6,308,249).

7. **As per claim 1**, Lee discloses a method for cycling through addresses of a memory device, comprising:

generating for each address a respective bit pattern comprised of a predetermined number of bits (pg. 129, 4th full paragraph; Fig. 5). *It should be noted that "cell" is analogous to "bit" and "data pattern of cell array/bake sequence" is analogous to "bit pattern." It should also be noted that each "data pattern/bake*

sequence" (Figs. 5(a)-(c)) comprised a predetermined number of programmed and erased cells.

Lee does not expressly disclose cycling through the respective bit pattern for each of the addresses with a transition of less than the predetermined number of bits for sequencing to each subsequent address.

Okazawa discloses cycling through the respective bit pattern for each of the addresses with a transition of less than the predetermined number of bits for sequencing to each subsequent address (col. 5, lines 24-39 and 53-67; Fig. 3; Fig. 4). *It should noted that "accessing" is analogous to "cycling." It should also be noted that Okazawa's grey code bit pattern requires only 16 bit transitions when accessing proceeds consecutively from the 1st address to the 32nd address as opposed to the binary bit pattern (i.e. the pattern that sequences to each subsequent address) which requires 32 bit transitions when accessing proceeds consecutively from the 1st address to the 32nd address.*

Lee and Okazawa are analogous art because they are from the same field of endeavor, that being accessing memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Okazawa's grey code bit pattern into Lee's bake sequence.

The motivation for doing so would have been so the processor can reduce the power consumption in the address terminal by decreasing the number of bit transitions in accessing to consecutive addresses of the memory by using address output of a grey code system (Okazawa, col. 6, lines 1-4).

Therefore, it would have been obvious to combine Lee and Okazawa for the benefit of obtaining the invention as specified in claim 1.

8. **As per claim 2**, the combination of Lee/Okazawa discloses cycling through the respective bit pattern for each of the addresses in a gray code sequence (Okazawa, col. 5, lines 9-17). *It should be noted that "grey code" is equivalent to "gray code."*

9. **As per claim 3**, the combination of Lee/Okazawa discloses the memory device is a flash memory device (Lee, pg. 128, Section III, 1st full paragraph, lines 1-3).

10. **As per claim 4**, the combination of Lee/Okazawa discloses eliminating charge gain failure of the flash memory device (Okazawa, col. 5, lines 9-17, 24-39 and 53-67; Lee, pg. 128, Section III, 1st full paragraph, lines 1-3). *It should be noted that this limitation fails to limit the scope of the invention but rather acts merely as an intended use of the invention. As recited on pg. 15, lines 18-20 in Applicant's specification, "because of such a small number of bit transitions for going to a subsequent address in cycling through each address of the flash 20 memory device 160, no charge gain failure occurs with the HTOL test system 200 of Fig. 9" it is clear that "eliminating charge gain failure of the flash memory device" is an advantage of the invention (intended use) rather than a limiting feature. Okazawa discloses using a small number of bit transitions for going to a subsequent address in cycling through each address of a memory device. That feature taken in combination with Lee's flash memory and it follows that that combination of Lee/Okazawa is* ***capable of*** *"eliminating charge gain failure of the flash memory device."*

11. **As per claim 5**, the combination of Lee/Okazawa discloses generating a respective binary bit pattern for each of the addresses (Okazawa, col. 3, lines 35-37; Fig. 1, element 1);

converting the respective binary bit pattern to a respective gray code bit pattern for each of the addresses (Okazawa, col. 3, lines 39-44; Fig. 1, element 2);

and using the respective gray code bit pattern by address decoders for accessing the memory device (Okazawa, col. 3, lines 44-46). *It should be noted that Okazawa does not explicitly show an "address decoder," however, it is inherently required within a computer system that some sort of "address decoder" interface between an address and memory in order to convert the address into the appropriate electrical signals for accessing the memory.*

12. **As per claim 6**, the combination of Lee/Okazawa discloses heating the memory device such that the step of cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device (Lee, pg. 129, 4th full paragraph, lines 5-6 and 9-10). *It should be noted that "cells baked at 250 °C for 24h" is analogous to "a test for HTOL."*

13. **As per claim 7**, the combination of Lee/Okazawa discloses cycling through the respective bit pattern for each of the addresses with a transition of a fixed number of bits for sequencing to each subsequent address (col. 5, lines 53-67; Fig. 4). *It should be noted as indicated by Fig. 4 the grey code bit pattern has a fixed number of bit transitions for sequencing to each subsequent address (that fixed number being 1).*

14. **As per claim 8**, the combination of Lee/Okazawa discloses the memory device is a flash memory device (Lee, pg. 128, Section III, 1st full paragraph, lines 1-3).

15. **As per claim 9**, the combination of Lee/Okazawa discloses eliminating charge gain failure of the flash memory device (Okazawa, col. 5, lines 9-17, 24-39 and 53-67; Lee, pg. 128, Section III, 1st full paragraph, lines 1-3). *Please see citation note for claim 4 above.*

16. **As per claim 10**, the combination of Lee/Okazawa discloses heating the memory device such that the step of cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device (Lee, pg. 129, 4th full paragraph, lines 5-6 and 9-10). *Please see the citation note for claim 6 above.*

17. **As per claim 11**, Lee discloses a system for cycling through addresses of a memory device, comprising:

an address generator for generating for each address a respective bit pattern comprised of a predetermined number of bits (pg. 129, 4th full paragraph; Fig. 5). *It should be noted that Lee does not explicitly disclose an "address generator," however, it is inherently required some sort of apparatus generated and changed the different "data patterns/bake sequences" during the HTOL test. Also, please see the citation note for the first limitation of claim 1 above.*

Lee does not expressly disclose means for cycling through the respective bit pattern for each of the addresses with a transition of less than the predetermined number of bits for sequencing to each subsequent address.

Okazawa discloses means for cycling through the respective bit pattern for each of the addresses with a transition of less than the predetermined number of bits for sequencing to each subsequent address (col. 5, lines 9-11, 24-39, and 53-67; Fig. 3; Fig. 4). *It should be noted that pg. 12, lines 27-29 of Applicant's specification appear to define this means as a "binary to gray code converter." Okazawa's "binary/grey conversion logic circuit" is equivalent to Applicant's "binary to gray code converter." Also, please see the citation note for the second limitation of claim 1 above.*

Lee and Okazawa are analogous art because they are from the same field of endeavor, that being accessing memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Okazawa's grey code bit pattern into Lee's bake sequence.

The motivation for doing so would have been so the processor can reduce the power consumption in the address terminal by decreasing the number of bit transitions in accessing to consecutive addresses of the memory by using address output of a grey code system (Okazawa, col. 6, lines 1-4).

Therefore, it would have been obvious to combine Lee and Okazawa for the benefit of obtaining the invention as specified in claim 11.

18. **As per claim 12**, the combination of Lee/Okazawa discloses a gray code converter for cycling through the respective bit pattern for each of the addresses in a gray code sequence (Okazawa, col. 5, lines 9-17). *It should be noted that "binary/grey conversion logic circuit" is analogous to "gray code converter." Also, please see the citation note for claim 2 above.*

19. **As per claim 13**, the combination of Lee/Okazawa discloses the memory device is a flash memory device (Lee, pg. 128, Section III, 1st full paragraph, lines 1-3).

20. **As per claim 14**, the combination of Lee/Okazawa discloses charge gain failure of the flash memory device is eliminated (Okazawa, col. 5, lines 9-17, 24-39 and 53-67; Lee, pg. 128, Section III, 1st full paragraph, lines 1-3). *Please see citation note for claim 4 above.*

21. **As per claim 15**, the combination of Lee/Okazawa discloses the address generator generates a respective binary bit pattern for each of the addresses, and wherein the gray code converter converts the respective binary bit pattern to a respective gray code bit pattern for each of the addresses (Okazawa, col. 3, lines 35-44; Fig. 1, elements 1 and 2), and wherein the system further comprises:

address decoders for decoding the respective gray code bit pattern for accessing the memory device (Okazawa, col. 3, lines 44-46). *Please see the citation notes for claim 5 above.*

22. **As per claim 16**, the combination of Lee/Okazawa discloses a heater for heating the memory device such that cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device (Lee, pg. 129, 4th full paragraph, lines 5-6 and 9-10). *It should be noted that it is inherently required that some sort of "heater" be used in order to bake the cells at a temperature of 250 °C for 24h.*

23. **As per claim 17**, the combination of Lee/Okazawa discloses means for cycling through the respective bit pattern for each of the addresses with a transition of a fixed

number of bits for sequencing to each subsequent address (col. 5, lines 9-11 and 53-67; Fig. 4). *It should be noted that pg. 12, lines 27-29 of Applicant's specification appear to define this means as a "binary to gray code converter." Okazawa's "binary/grey conversion logic circuit" is equivalent to Applicant's "binary to gray code converter." Also, please see the citation note for claim 7 above.*

24. **As per claim 18**, the combination of Lee/Okazawa discloses the memory device is a flash memory device (Lee, pg. 128, Section III, 1st full paragraph, lines 1-3).

25. **As per claim 19**, the combination of Lee/Okazawa discloses charge gain failure of the flash memory device is eliminated (Okazawa, col. 5, lines 9-17, 24-39 and 53-67; Lee, pg. 128, Section III, 1st full paragraph, lines 1-3). *Please see citation note for claim 4 above.*

26. **As per claim 20**, the combination of Lee/Okazawa discloses a heater for heating the memory device such that cycling through the respective bit pattern for each of the addresses is performed during a test for HTOL (high temperature operating life) of the memory device (Lee, pg. 129, 4th full paragraph, lines 5-6 and 9-10). *Please see the citation notes for both claims 6 and 16 above.*

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-20** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,450,363 discloses gray coding for a multilevel cell memory system.

2. U.S. Patent 5,630,086 discloses memory control circuitry is provided which includes circuitry for generating a sequence of gray code values.

3. U.S. Patent 5,987,574 discloses a memory controller that arbitrates requests for access to the memory such that, if possible, sequential memory accesses are directed to alternating memory banks.

4. U.S. Patent 6,549,479 discloses a dynamic random access memory device uses a gray code counter to generate addresses in a self-refresh operating mode so that only one bit of a row address generated by the counter changes state from one refresh cycle to the next.

5. Non-patent literature, Brand et al., "Novel Read Disturb Failure Mechanism Induced by FLASH Cycling", 1993, Reliability Physics Symposium, 31st Annual Proceedings, IEEE International, pp. 127-132.

6. Non-patent literature, Fastow et al., "Bake Induced Charge Gain in NOR Flash Cells", April 2000, IEEE Electronic Device Letters, Vol. 21, No. 4, pp. 184-186.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
May 1, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER